REMARKS

Prior to the present amendment, claims 1-20 were pending in the present application. By the present amendment, claims 1, 11, 15, and 20 have been amended and claims 13 and 14 have been canceled. Thus, claims 1-12 and 15-20 remain in the present application. Reconsideration and allowance of outstanding claims 1-12 and 15-20 in view of the above amendments and the following remarks are respectfully requested.

A. Rejection of Claims 1-20 under 35 USC §103(a)

The Examiner has rejected claims 1-20 under 35 USC §103(a) as being unpatentable over U.S. patent application publication number 2004/0239487 to Russell Hershbarger (hereinafter "Hershbarger") in view of U.S. patent application publication number 2003/0215020 to Dong et al. (hereinafter "Dong"). For the reasons discussed below, Applicants respectfully submit that the present invention, as defined by amended independent claims 1 and 11, is patentably distinguishable over Hershbarger and Dong, either singly or in combination thereof.

The present invention, as defined by amended independent claim 1, recites, among other things, a system side device configured to generate an amplitude modulated clock signal when the system side device is in a transmit mode and further configured to generate an unmodulated clock signal when the system side device is in a receive mode, and a line side device configured to cause the unmodulated clock signal to be amplitude modulated when the system side device is in the receive mode by varying an impedance

of a controlled impedance module. As disclosed in the present application, when a system side device is in a receive mode and a line side device is in a transmit mode, power-clock drivers in the system side device transmit only unmodulated clock signals to provide clock and power to the line side device through a transformer. As also disclosed in the present application, the unmodulated clock signals are amplitude modulated by the line side device by varying the impedance of a controlled impedance module.

As further disclosed in the present application, when the system side device is in a transmit mode and the line side device is in a receive mode, the power-clock drivers provide amplitude modulated clock signals to the line side device through the transformer. Since the present invention uses a single path through a transformer to provide power, clock, and bi-directional data transfer, noise and ground voltage surges occurring in the line side device are substantially prevented from passing through to the system side device. Also, since capacitors are no longer part of the data transfer mechanism, the line side device can be placed at a substantially greater distance away from the system side device, which advantageously increases design flexibility of systems base on the invention's digital isolation barrier.

In contrast to the present invention as defined by amended independent claim 1, Hershbarger does not teach, disclose, or suggest a system side device configured to generate an amplitude modulated clock signal when the system side device is in a transmit mode and further configured to generate an unmodulated clock signal when the system side device is in a receive mode, and a line side device configured to cause the

unmodulated clock signal to be amplitude modulated when the system side device is in the receive mode by varying an impedance of a controlled impedance module. Hershbarger specifically discloses Host 150 connected to PSTN (public switched telephone network) 160 via DAA 100, which includes Host Interface Component (HIC) 104, isolation barrier 106, Line Interface Component (LIC) 108, and External Circuitry 110. See, for example, page 2, paragraph [0038] and Figure 1 of Hershbarger.

In Hershbarger, encoded data is transmitted from LIC to HIC 104 over the barrier (i.e. isolation barrier 106) using impedance modulation. See, for example, Hershbarger, page 4, paragraph [0056]. However, Hershbarger fails to teach, disclose, or suggest a line side device configured to cause an unmodulated clock signal to be amplitude modulated when the system side is in a receive mode by varying an impedance of a controlled impedance module, as specified in amended independent claim 1. In Hershbarger, a digital sigma-delta modulator takes the output of transmit interpolation filters as input and generates a bit stream that feeds into MSBI 230 for time-multiplexing with control data and double-balanced encoding prior to transmission (from HIC 104) across the barrier (i.e. barrier 106) to LIC 108. See, for example, Hershbarger, page 4, paragraph [0055]. However, Hershbarger fails to teach, disclose, or remotely suggest a system side device configured to generate an amplitude modulated clock signal when the system side device is in a transmit mode and further configured to generate an unmodulated clock signal when the system side device is in a receive mode, as specified by amended independent

claim 1. Furthermore, Hershbarger provides no motivation for using amplitude modulation to modulate a clock signal.

In contrast to the present invention as defined by amended independent claim 1, Dong does not teach, disclose, or suggest a system side device configured to generate an amplitude modulated clock signal when the system side device is in a transmit mode and further configured to generate an unmodulated clock signal when the system side device is in a receive mode, and a line side device configured to cause the unmodulated clock signal to be amplitude modulated when the system side device is in the receive mode by varying an impedance of a controlled impedance module. Dong specifically discloses input signal 21 coupled to modulator 22 and modulator 22 coupled to demodulator 26 via HF transformer 24. See, for example, page 2, paragraph [0026] and Figure 2 of Dong. Dong teaches that simple amplitude modulation can be used in modulator 22 to modulate input signal 21. See, for example, Dong, page 2, paragraph [0026].

Dong states that although input signal 21 may be either digital or analog, the signal presented to HF transformer 24 is an analog signal. See, for example, Dong, page 2, paragraph [0026]. However, Dong fails to teach, disclose, or suggest a system side device configured to generate an amplitude modulated clock signal when the system side device is in a transmit mode and further configured to generate an unmodulated clock signal when the system side device is in a receive mode, and a line side device configured to cause the unmodulated clock signal to be amplitude modulated when the system side device is in the receive mode by varying an impedance of a controlled impedance module,

as specified by amended independent claim 1. Thus, Dong fails to cure the basic deficiencies of Hershbarger discussed above.

On page 3 of the Office Action dated October 18, 2005, the Examiner states that "[i]t would have been obvious to one of ordinary skill in the art at the time of the invention to replace a pulse transmitter and pulse transformer with the high-frequency transmitter and high-frequency transformer as taught by Dong for the purpose of reducing costs and enabling linear data transmission. However, in Hershbarger, a digital signal is transmitted across an isolation barrier (e.g. isolation barrier 106). In contrast, the signal presented to HF transformer 24 (i.e. an isolation barrier) in Dong is an analog signal. Thus, Hershbarger and Dong present two completely different methods of transferring data across an isolation barrier. As such, the method and apparatus for full duplex signaling across a transformer would have to be substantially altered to incorporate amplitude modulation as taught by Dong. Thus, Applicants respectfully submit that there is insufficient motivation for one skilled in the art to combine Hershbarger and Dong as suggested by the Examiner.

For the foregoing reasons, Applicants respectfully submit that the present invention, as defined by amended independent claim 1, is not taught, disclosed, or suggested by Hershbarger and Dong, either singly or in combination thereof. Thus, amended independent claim 1 is patentably distinguishable over Hershbarger and Dong and, as such, claims 2-10 depending from amended independent claim 1 are, *a fortiori*,

also patentably distinguishable over Hershbarger and Dong for at least the reasons presented above and also for additional limitations contained in each dependent claim.

Also, amended independent claim 11 recites similar limitations as amended independent claim 1. Thus, for similar reasons as discussed above, amended independent claim 11 is also patentably distinguishable over Hershbarger and Dong. As such, claims 12 and 15-20 depending from amended independent claim 11 are, *a fortiori*, also patentably distinguishable over Hershbarger and Dong for at least the reasons presented above and also for additional limitations contained in each dependent claim.

B. Conclusion

Based on the foregoing reasons, the present invention, as defined by amended independent claims 1 and 11 and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 1-12 and 15-20 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of claims 1-12 and 15-20 pending in the present application is respectfully requested.

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Respectfully Submitted,
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